WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device comprising the consecutive steps of:

depositing a metallic conductive film on an underlying insulating film;

consecutively depositing first and second insulator films on said metallic conductive film;

patterning said first and second insulator films to have a substantially same patterned area;

etching said second insulator film selectively from said first insulator film to configure said second insulator film to have a width smaller than a width of said first insulator film;

patterning said metallic conductive film by using said first and second insulator films as an etching mask;

depositing a third insulator film on said first and second insulator films and said underlying insulating film;

etching-back said third insulator film to configure a side-wall film covering at least said patterned metallic conductive film; and

depositing a fourth insulator film to embed therein said side-wall oxide film on said underlying oxide film.

2. The method according to claim 1, wherein said etching-back step configures said side-wall oxide film to have a tapered mesa structure

having a larger width toward a bottom thereof.

3. The method according to claim 1, further comprising, after said fourth insulator film depositing step, the steps of etching said fourth insulator film to form therein a contact hole by using said side-wall film as an etch stopper, and forming a contact plug in said contact hole.

4. The method according to claim 1, wherein said first and second insulator films are a silicon nitride film and a silicon oxide film, respectively.

5. The method according to claim 1, wherein said method fabricates a semiconductor memory device.

6. A method for fabricating a semiconductor device comprising the consecutive steps of:

depositing a metallic conductive film on an underlying insulating film;

consecutively depositing first and second insulator films on said metallic conductive film;

patterning said first and second insulator films to have a substantially same patterned area;

patterning said metallic conductive film by using said first and second insulator films as an etching mask;

etching said second insulator film selectively from said first insulator

film to configure said second insulator film to have a width smaller than a width of said first insulator film;

depositing a third insulator film on said first and second insulator films and said underlying insulating film;

etching-back said third insulator film to configure a side-wall film covering at least said patterned metallic conductive film; and

depositing a fourth insulator film to embed therein said side-wall oxide film on said underlying oxide film.

7. The method according to claim 6, wherein said etching-back step configures said side-wall oxide film to have a tapered mesa structure having a larger width toward a bottom thereof.

8. The method according to claim 6, further comprising, after said fourth insulator film depositing step, the steps of etching said fourth insulator film to form therein a contact hole by using said side-wall film as an etch stopper, and forming a contact plug in said contact hole.

9. The method according to claim 6, wherein said first and second insulator films are a silicon nitride film and a silicon oxide film, respectively.

10. The method according to claim 6, wherein said method fabricates a semiconductor memory device.